OIPE IAP20
JUL 16 2007
PATENT & TRADEMARK OFFICE

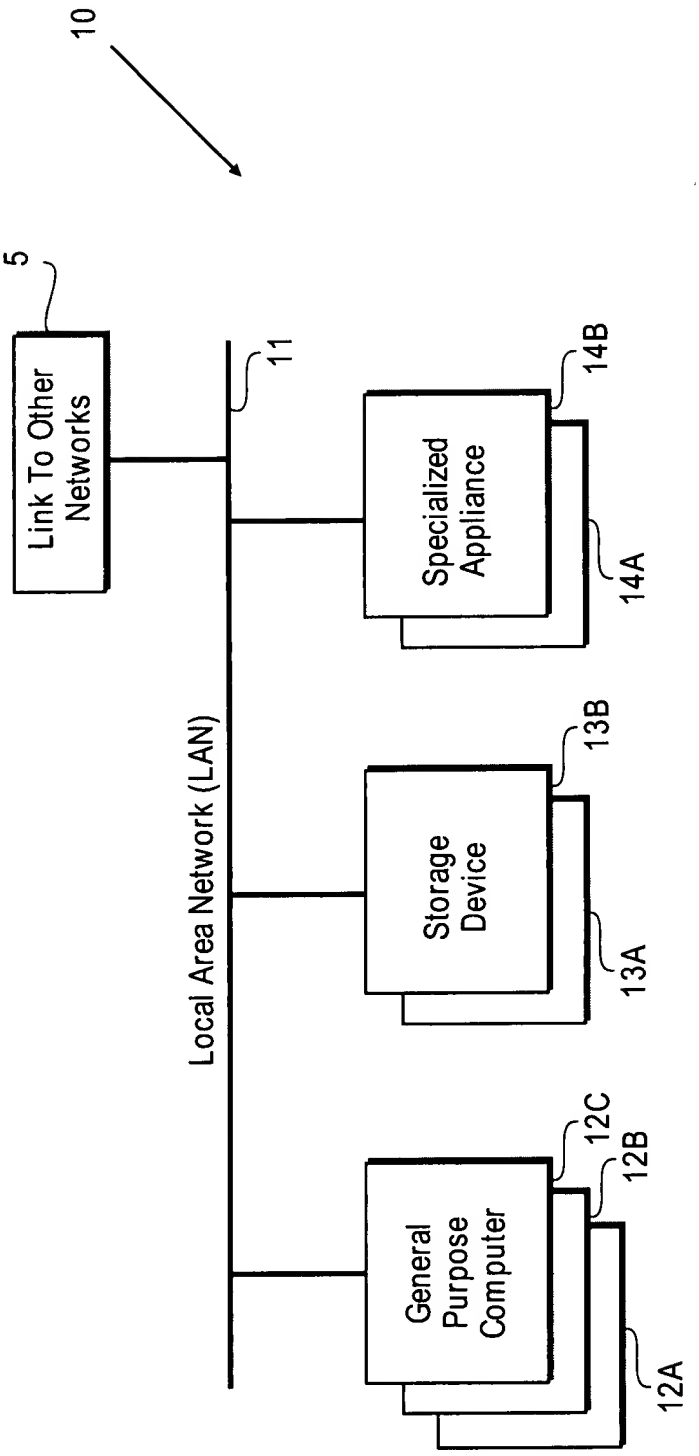


FIG. 1
(Prior Art)
Local Area Network (LAN) Abstract View

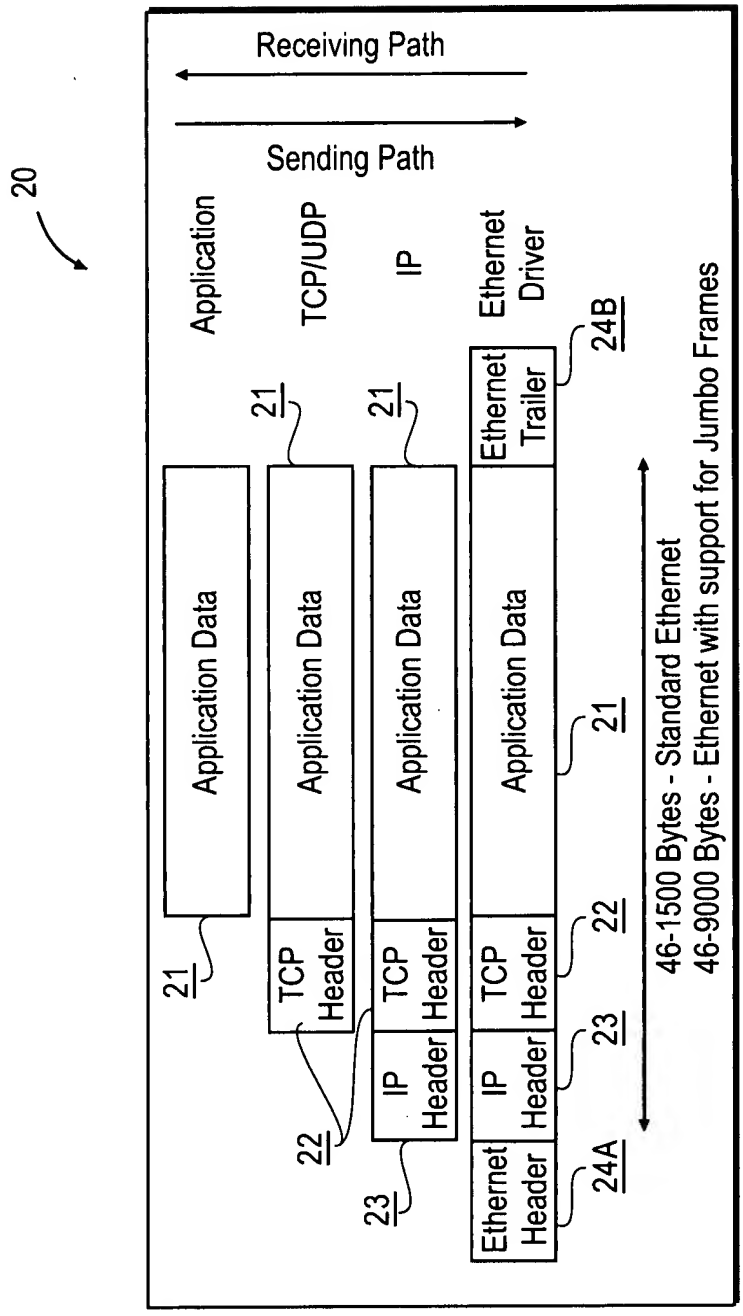


FIG. 2
(Prior Art) Data Encapsulation Through The Network Stack

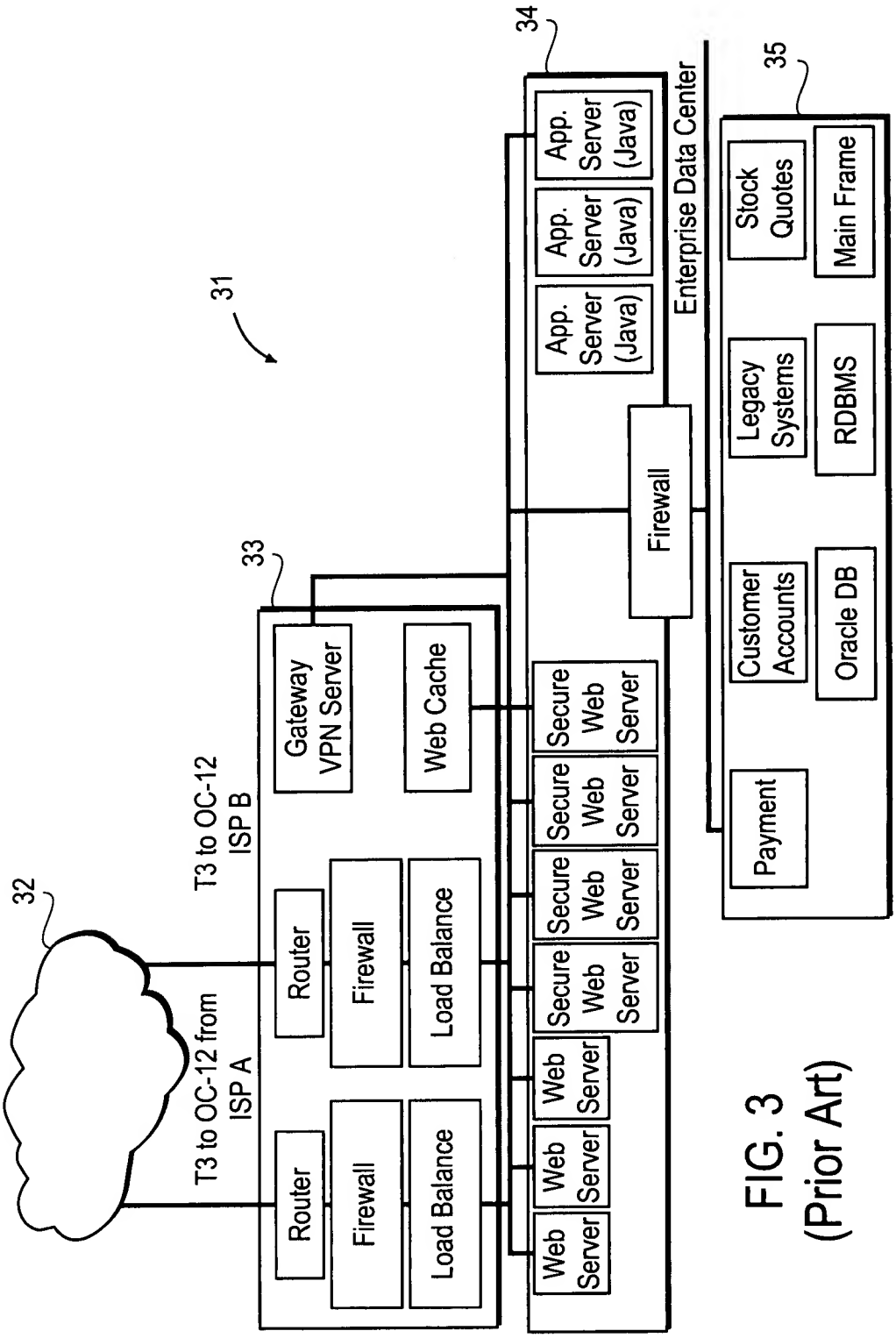


FIG. 3
(Prior Art)

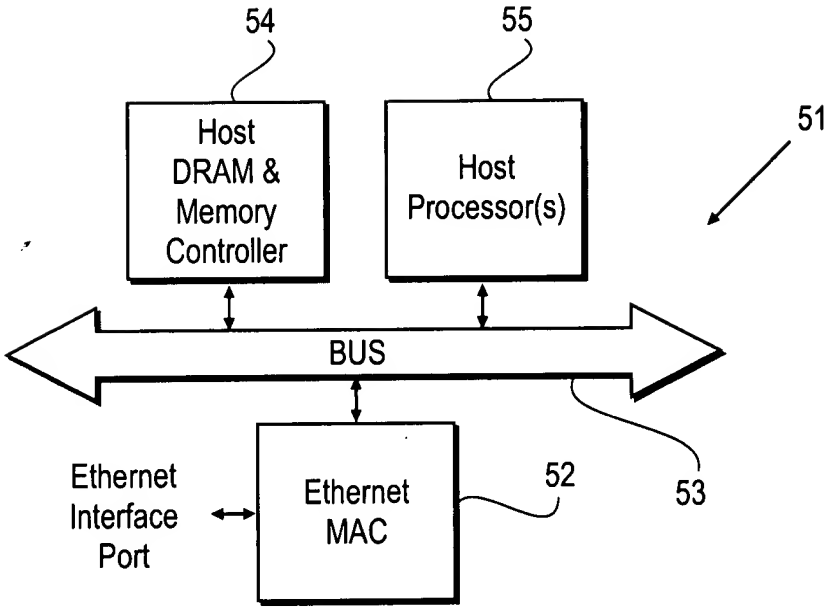


FIG. 4
(Prior Art)

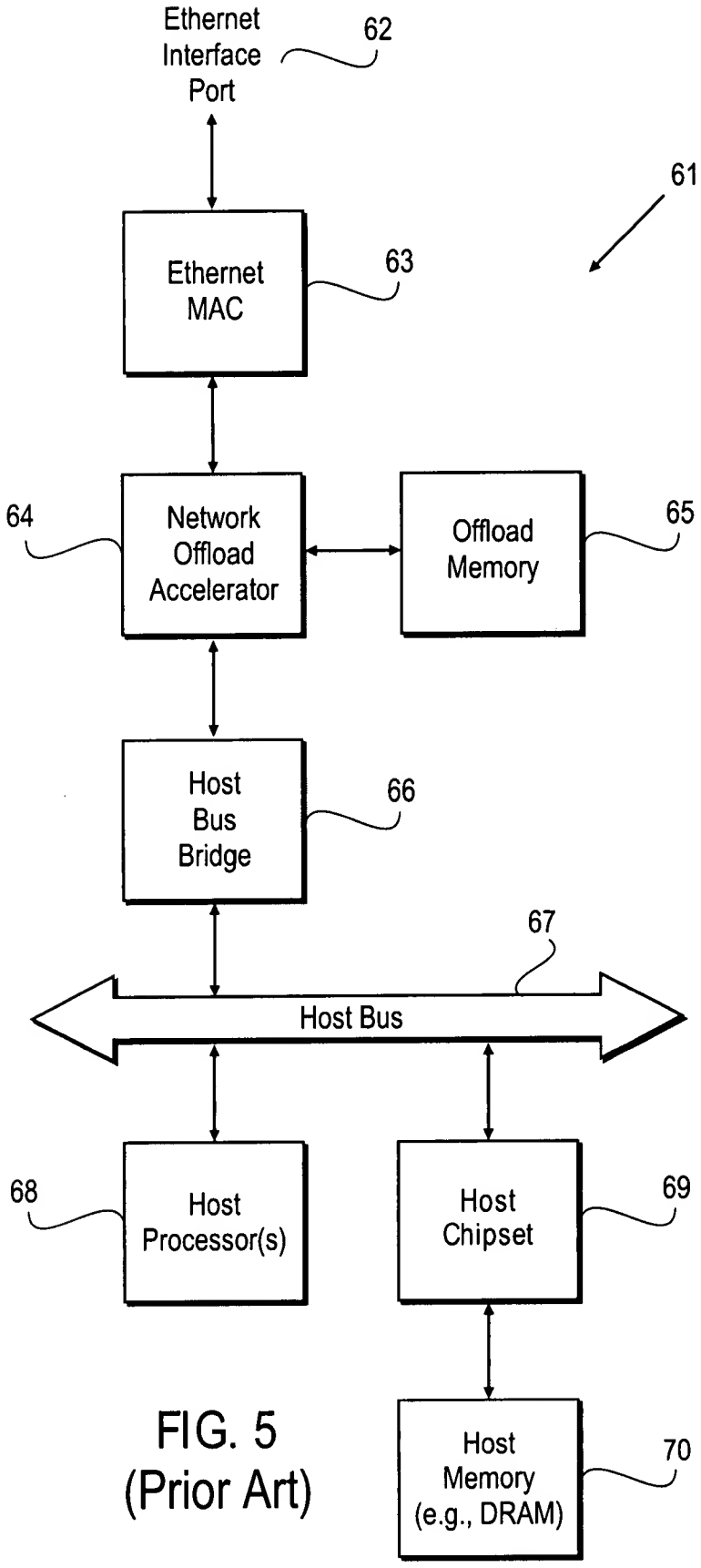


FIG. 5
(Prior Art)

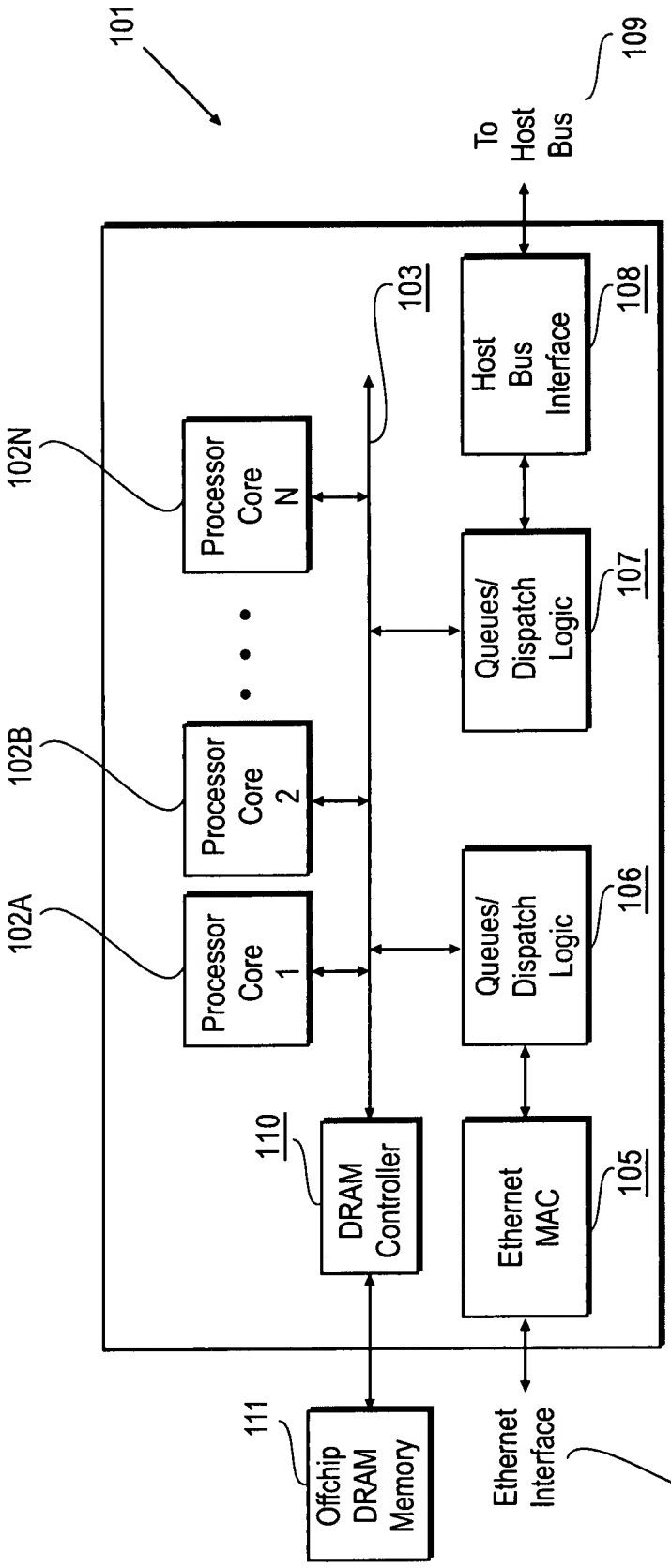


FIG. 6A Block Diagram of Network Protocol Offload Chip

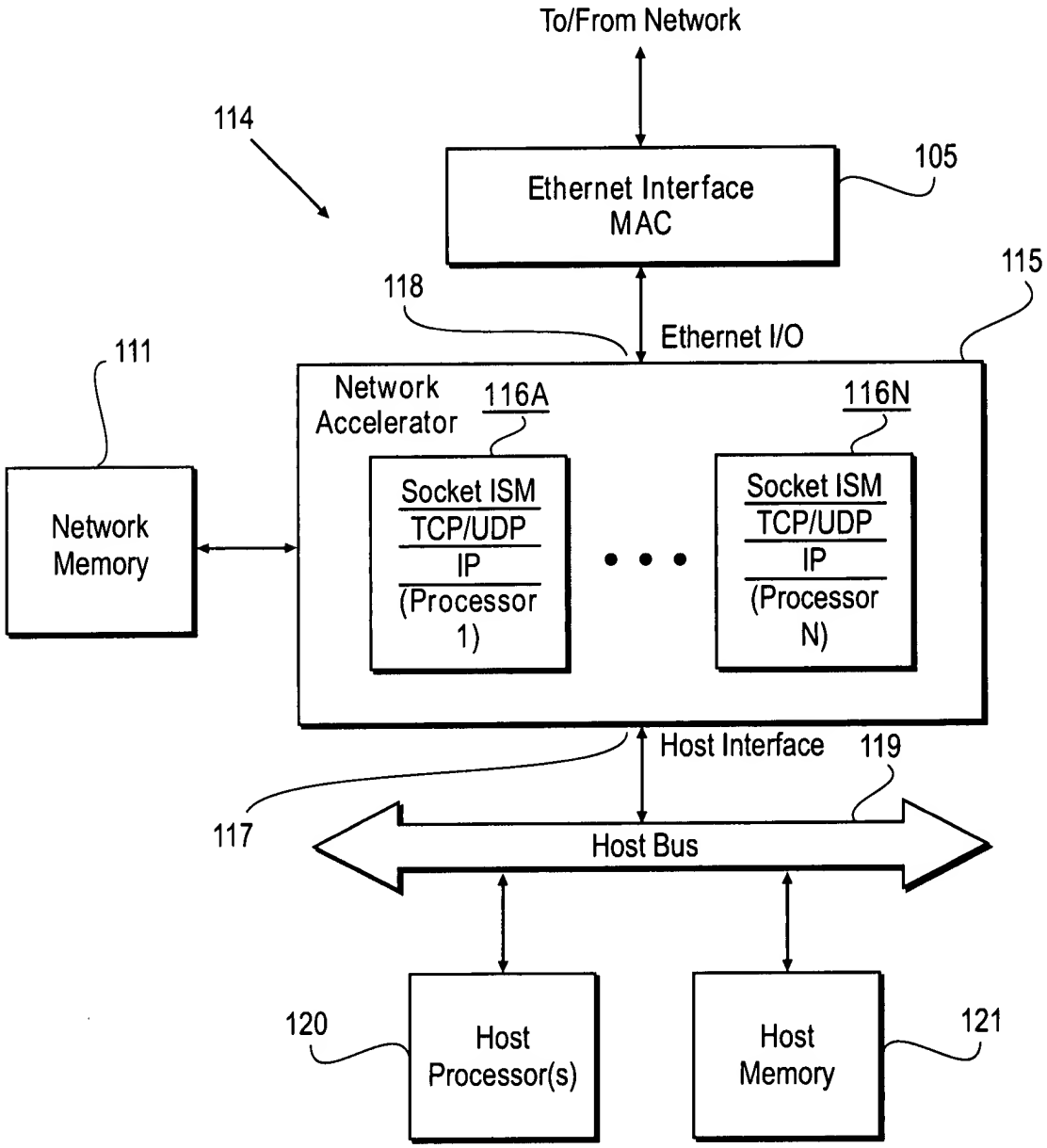

To/From Network
114
Ethernet Interface MAC
105
115
118
Ethernet I/O
111
Network Accelerator
116A
116N
Network Memory
Socket ISM
TCP/UDP
IP
(Processor 1)
Socket ISM
TCP/UDP
IP
(Processor N)
Host Interface
119
117
Host Bus
120
Host Processor(s)
Host Memory
121

FIG. 6B

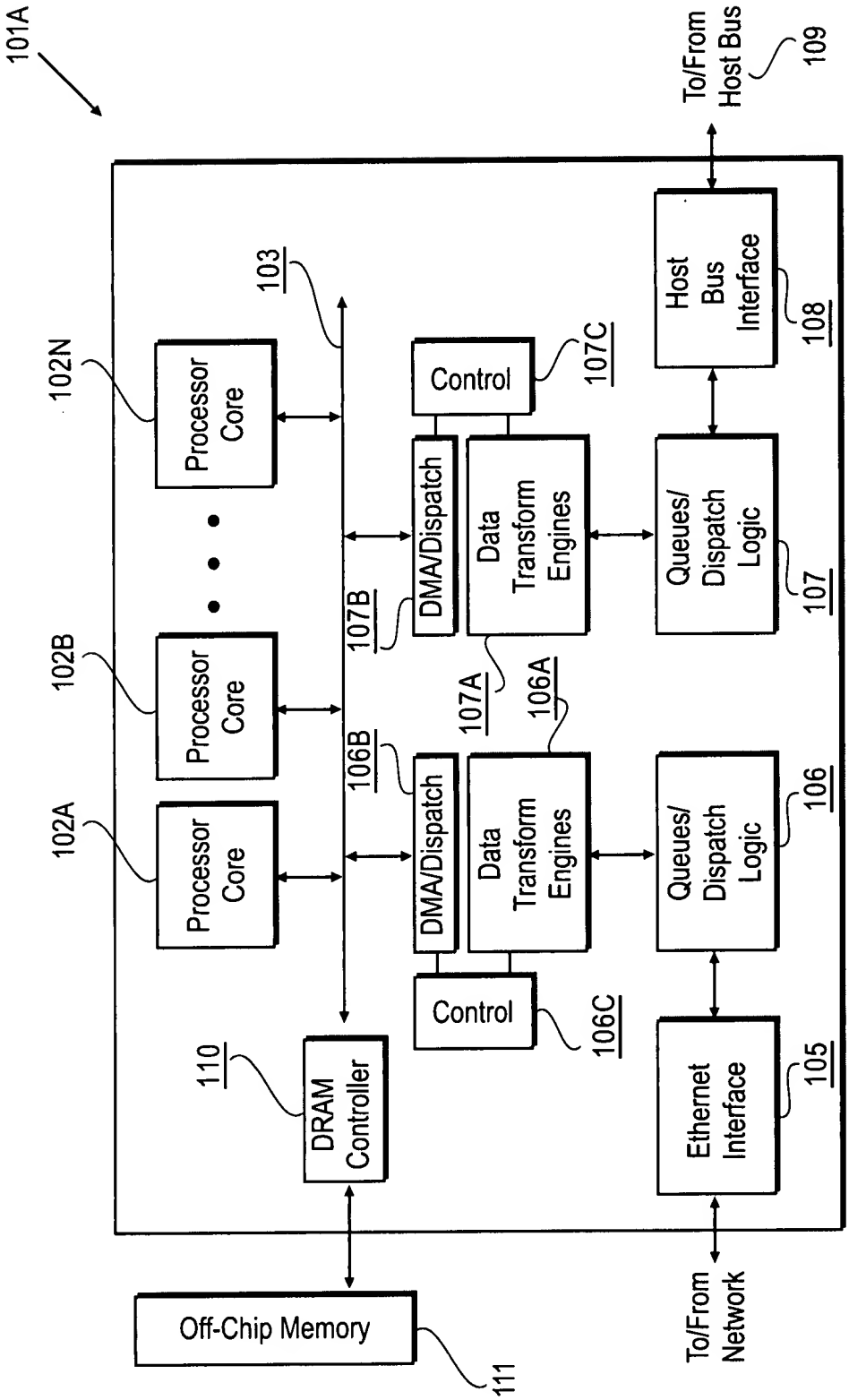


FIG. 6C Block Diagram of Data Transform Acceleration

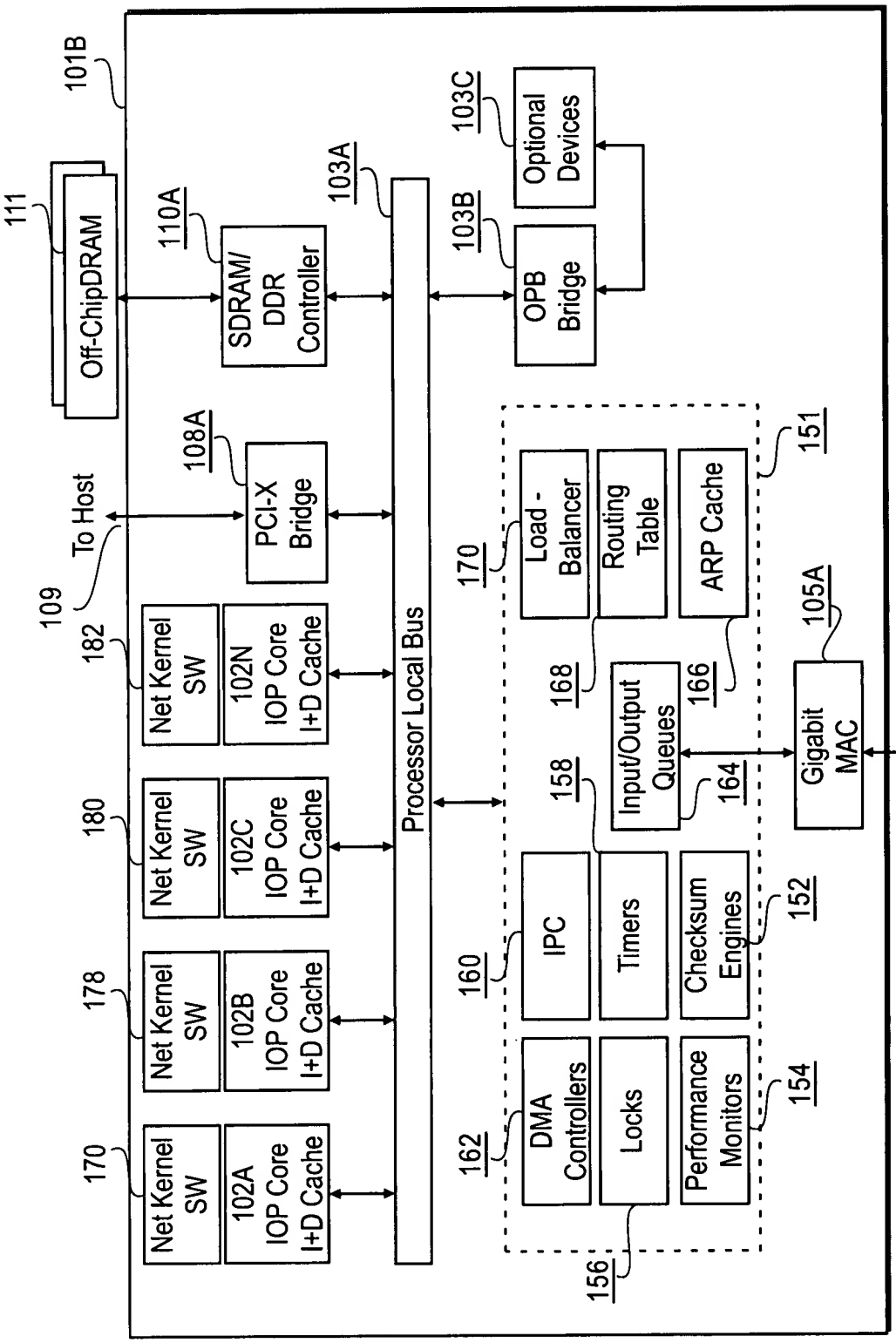

101B
111
Off-ChipDRAM
110A
SDRAM/
DDR
Controller
103A
103C
Optional
Devices
103B
OPB
Bridge
108A
PCI-X
Bridge
To Host
109
182
Net Kernel
SW
102N
IOP Core
I+D Cache
180
Net Kernel
SW
102C
IOP Core
I+D Cache
178
Net Kernel
SW
102B
IOP Core
I+D Cache
170
Net Kernel
SW
102A
IOP Core
I+D Cache
Processor Local Bus
170
Load -
Balancer
Routing
Table
ARP Cache
151
168
166
Input/Output
Queues
158
164
IPC
Timers
Checksum
Engines
152
160
162
DMA
Controllers
Locks
Performance
Monitors
154
156
Gigabit
MAC
105A
To/From Network
104

FIG. 7

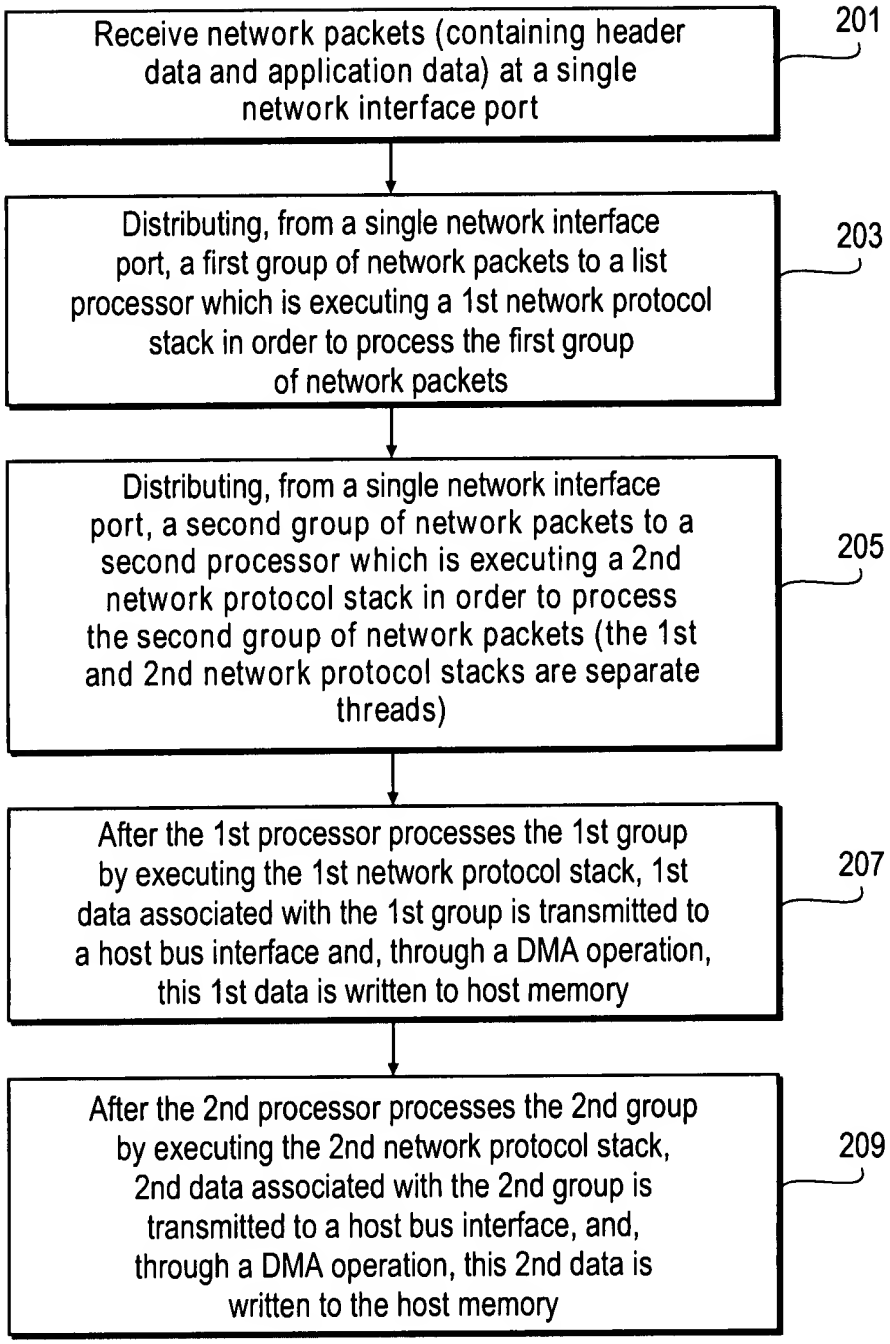

Receive network packets (containing header data and application data) at a single network interface port
201
Distributing, from a single network interface port, a first group of network packets to a list processor which is executing a 1st network protocol stack in order to process the first group of network packets
203
Distributing, from a single network interface port, a second group of network packets to a second processor which is executing a 2nd network protocol stack in order to process the second group of network packets (the 1st and 2nd network protocol stacks are separate threads)
205
After the 1st processor processes the 1st group by executing the 1st network protocol stack, 1st data associated with the 1st group is transmitted to a host bus interface and, through a DMA operation, this 1st data is written to host memory
207
After the 2nd processor processes the 2nd group by executing the 2nd network protocol stack, 2nd data associated with the 2nd group is transmitted to a host bus interface, and, through a DMA operation, this 2nd data is written to the host memory
209

FIG. 8A

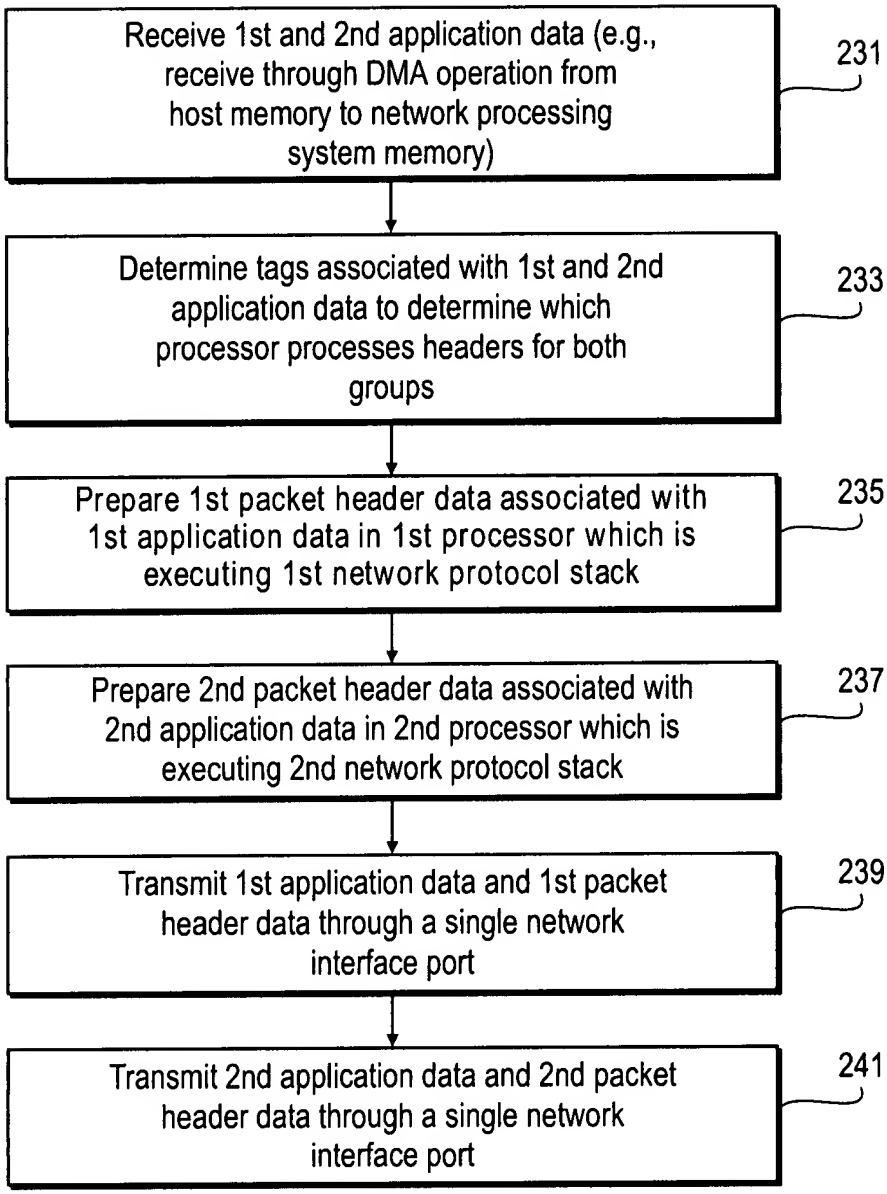

Receive 1st and 2nd application data (e.g., receive through DMA operation from host memory to network processing system memory)
231
Determine tags associated with 1st and 2nd application data to determine which processor processes headers for both groups
233
Prepare 1st packet header data associated with 1st application data in 1st processor which is executing 1st network protocol stack
235
Prepare 2nd packet header data associated with 2nd application data in 2nd processor which is executing 2nd network protocol stack
237
Transmit 1st application data and 1st packet header data through a single network interface port
239
Transmit 2nd application data and 2nd packet header data through a single network interface port
241

FIG. 8B

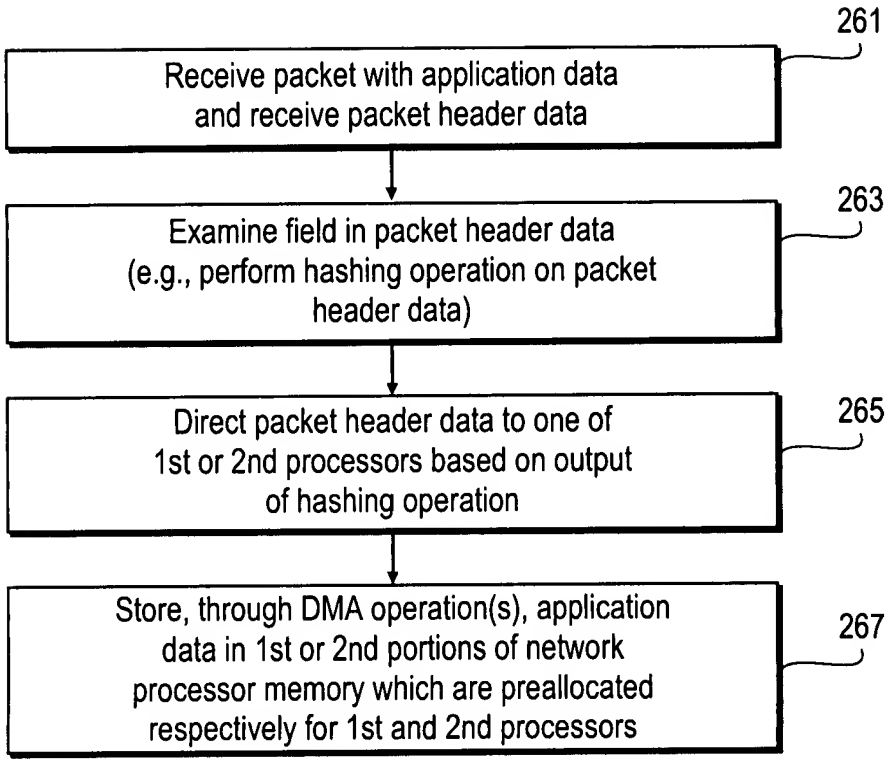

261
Receive packet with application data and receive packet header data
263
Examine field in packet header data (e.g., perform hashing operation on packet header data)
265
Direct packet header data to one of 1st or 2nd processors based on output of hashing operation
267
Store, through DMA operation(s), application data in 1st or 2nd portions of network processor memory which are preallocated respectively for 1st and 2nd processors

FIG. 8C

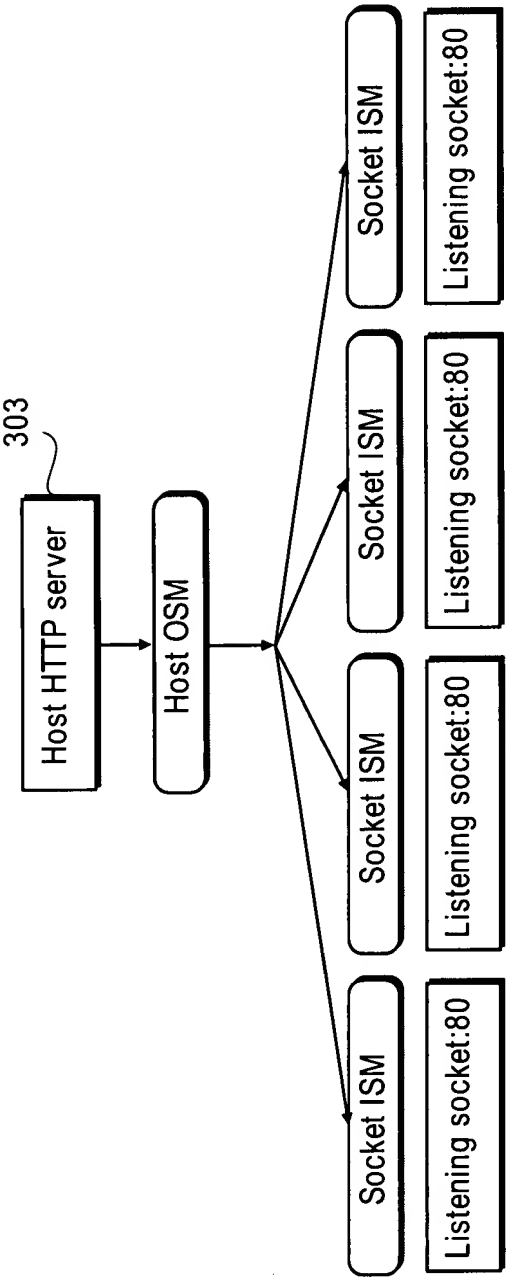

303
Host HTTP server
Host OSM
Socket ISM
Listening socket:80
Socket ISM
Listening socket:80
Socket ISM
Listening socket:80
Socket ISM
Listening socket:80
Replication of listening sockets

FIG. 9A

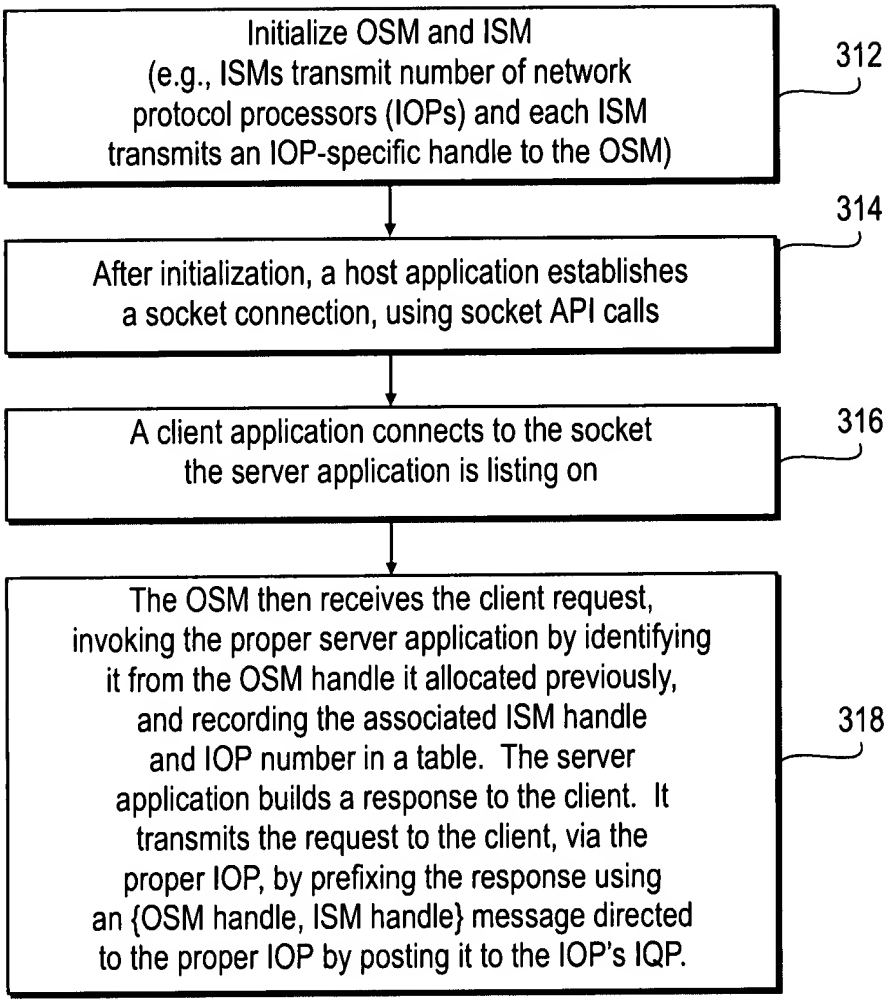

Initialize OSM and ISM (e.g., ISMs transmit number of network protocol processors (IOPs) and each ISM transmits an IOP-specific handle to the OSM)
312
After initialization, a host application establishes a socket connection, using socket API calls
314
A client application connects to the socket the server application is listing on
316
The OSM then receives the client request, invoking the proper server application by identifying it from the OSM handle it allocated previously, and recording the associated ISM handle and IOP number in a table. The server application builds a response to the client. It transmits the request to the client, via the proper IOP, by prefixing the response using an {OSM handle, ISM handle} message directed to the proper IOP by posting it to the IOP's IQP.
318

FIG. 9B

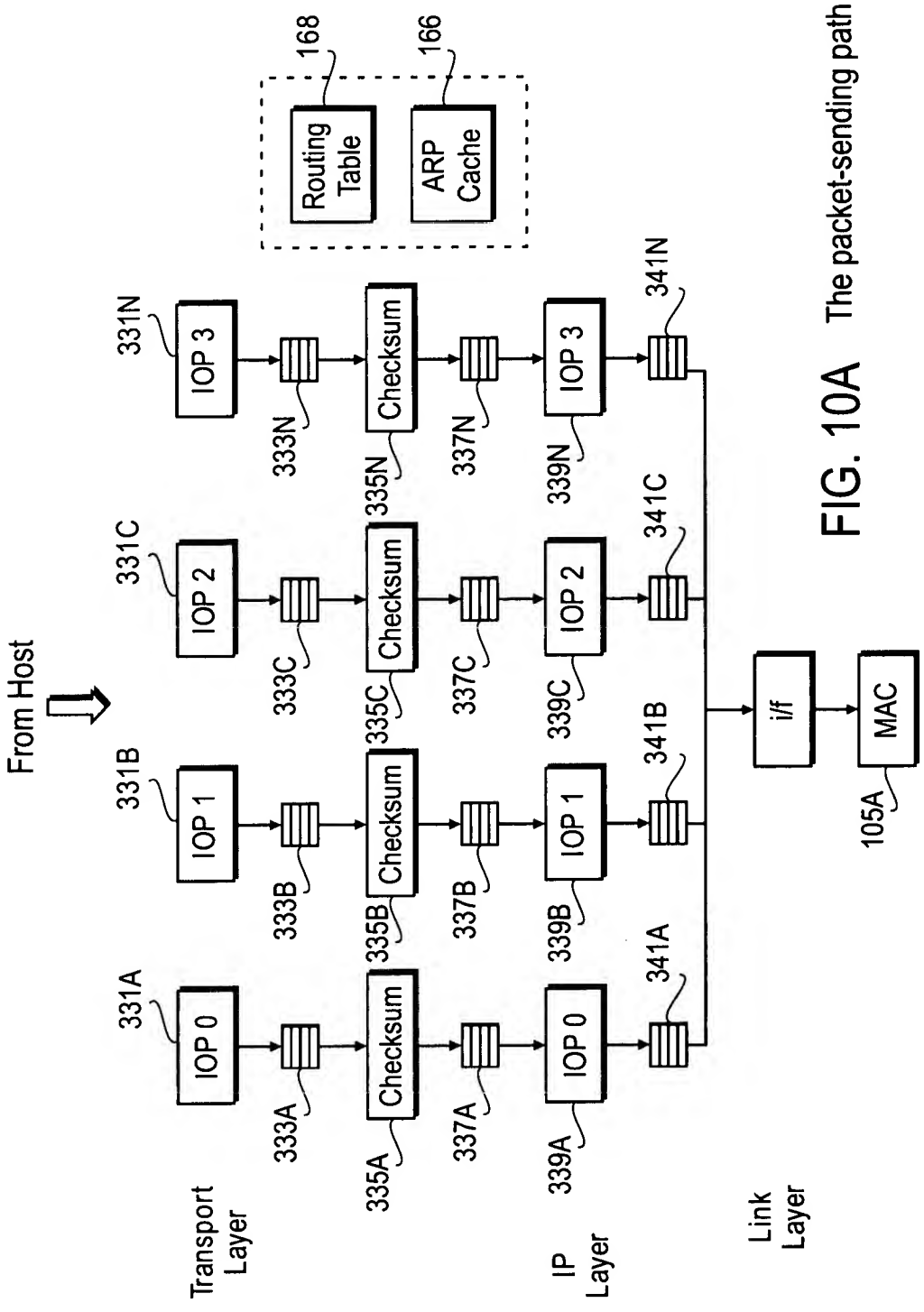


FIG. 10A The packet-sending path

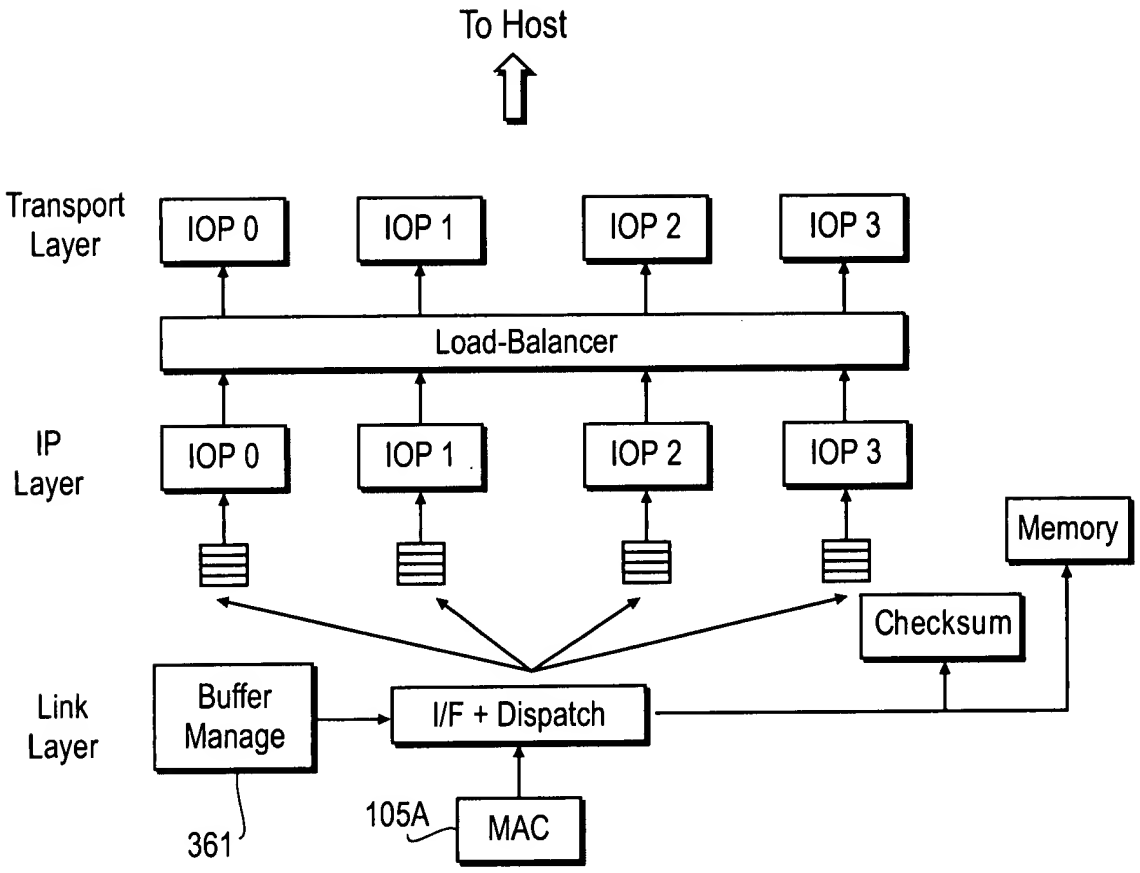


FIG. 10B The packet-receiving path

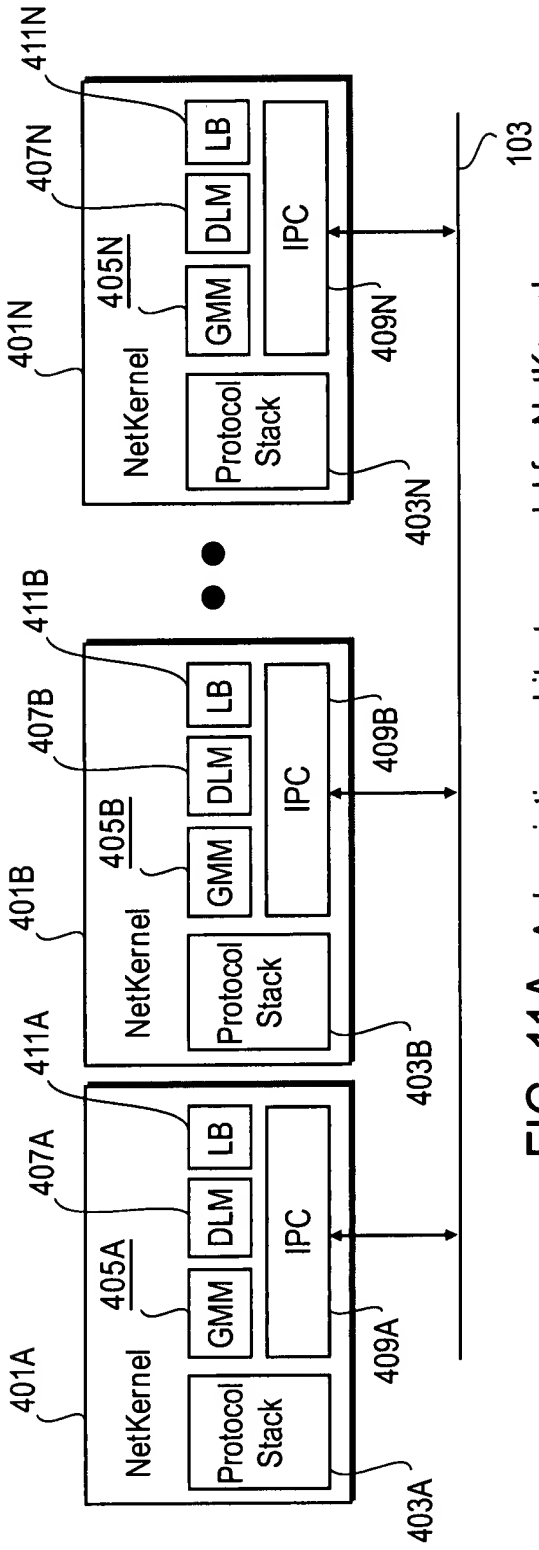


FIG. 11A A descriptive architecture model for NetKernel

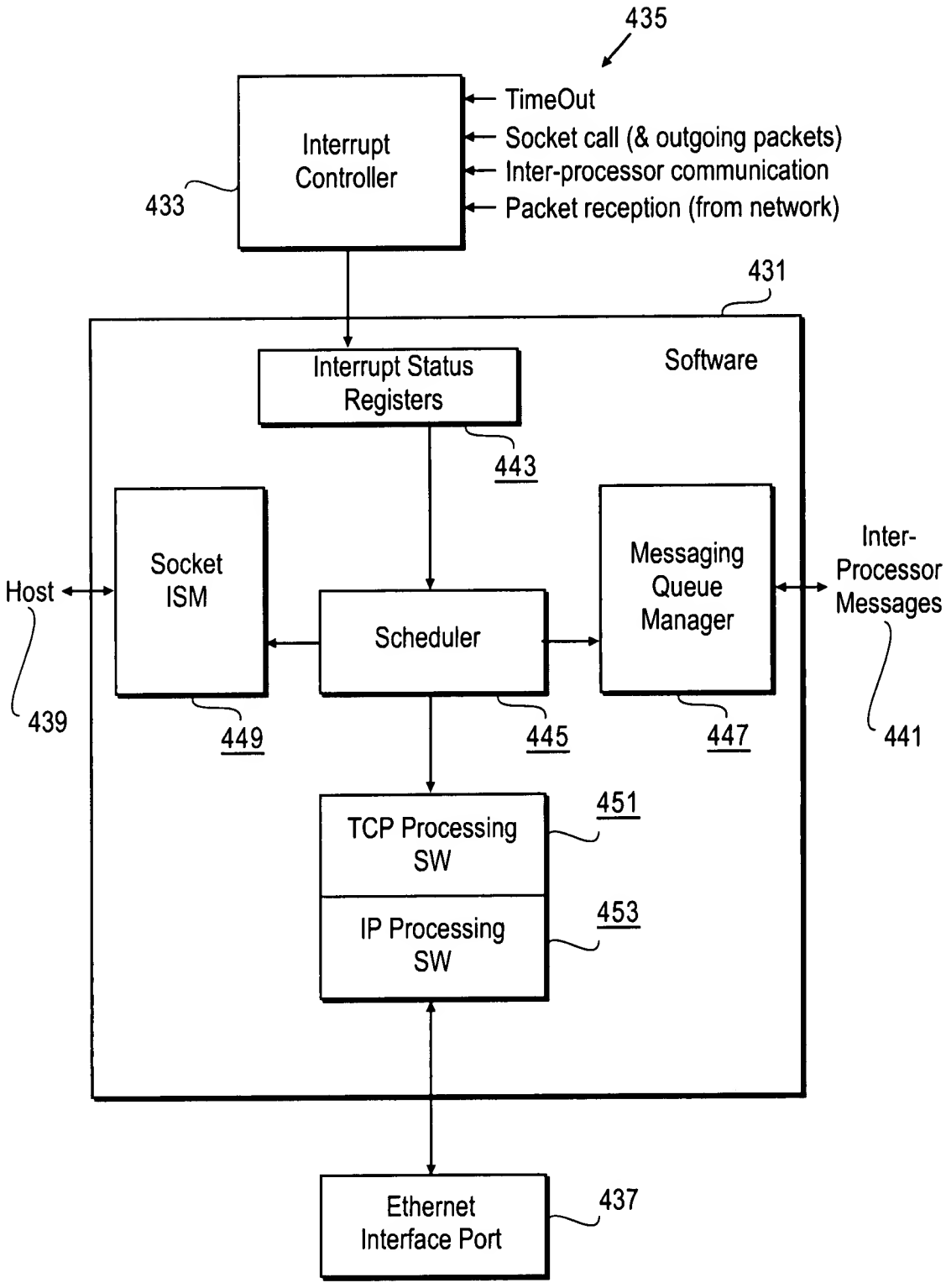

435
Interrupt Controller
433
TimeOut
Socket call (& outgoing packets)
Inter-processor communication
Packet reception (from network)
431
Software
Interrupt Status Registers
443
Socket ISM
Host
439
Scheduler
Messaging Queue Manager
Inter-Processor Messages
441
449
445
447
TCP Processing SW
451
IP Processing SW
453
Ethernet Interface Port
437

FIG. 11B

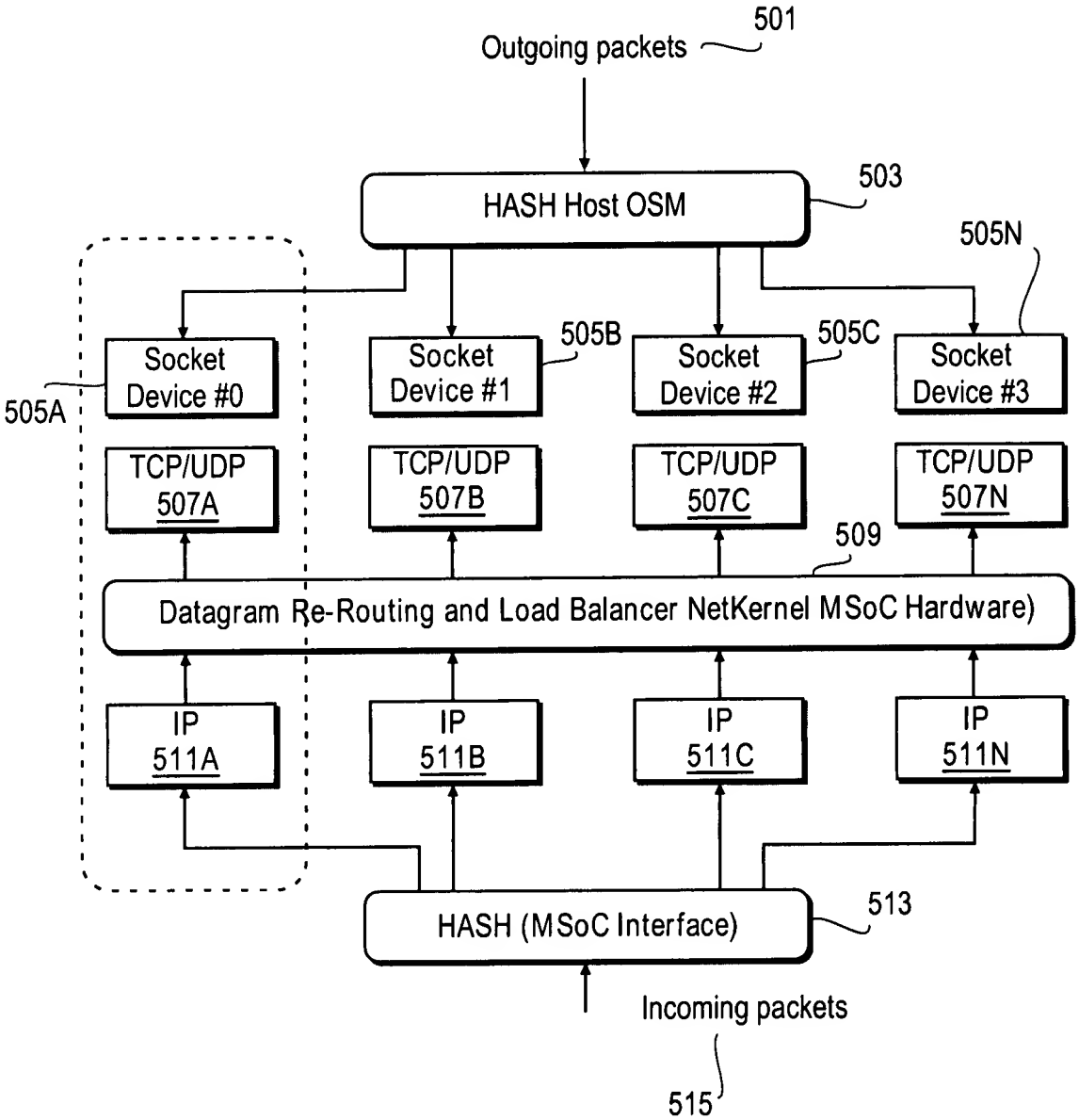


FIG. 12A

An illustration of packet flows for load balancing

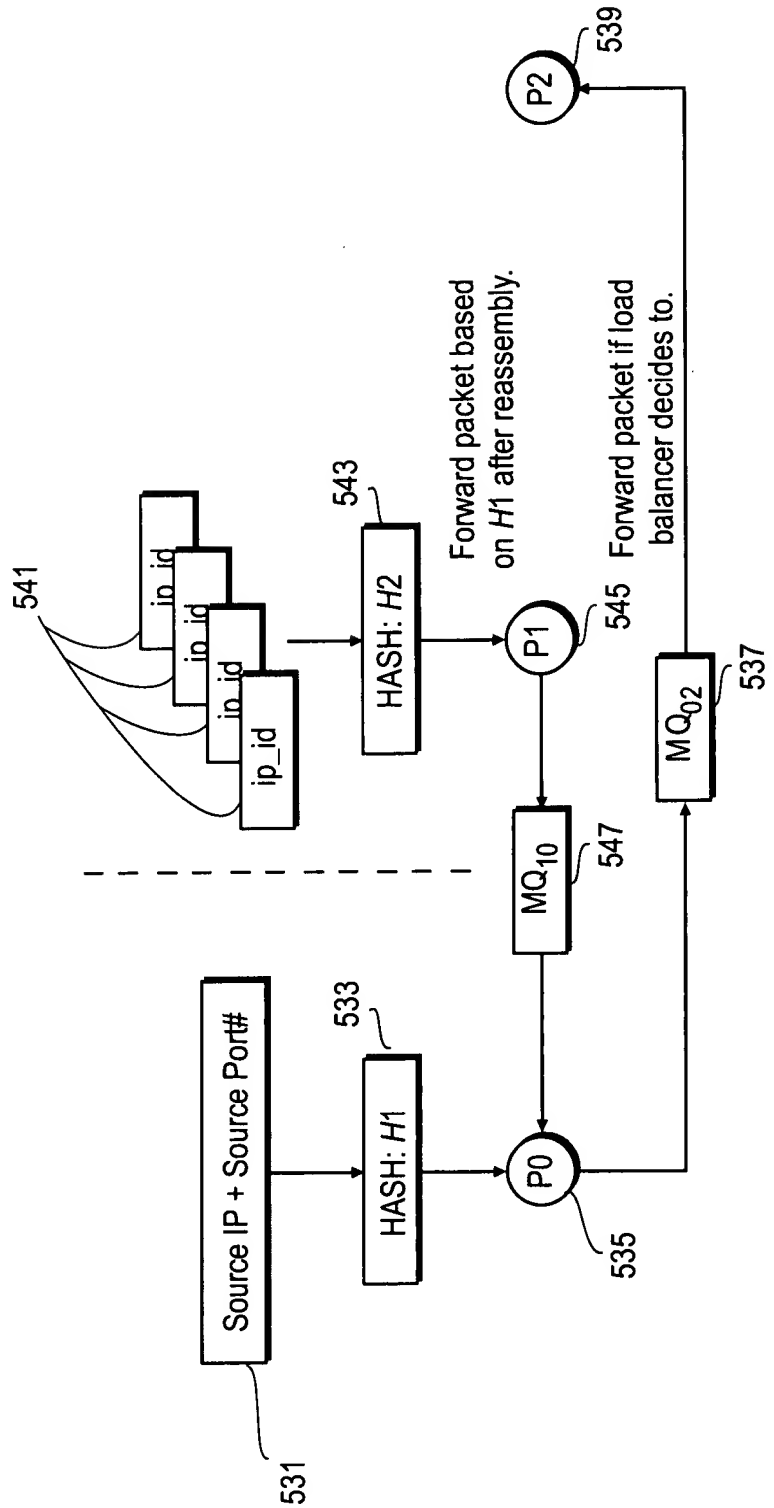


FIG. 12B Illustration of directing packets on address hashing and load balancing

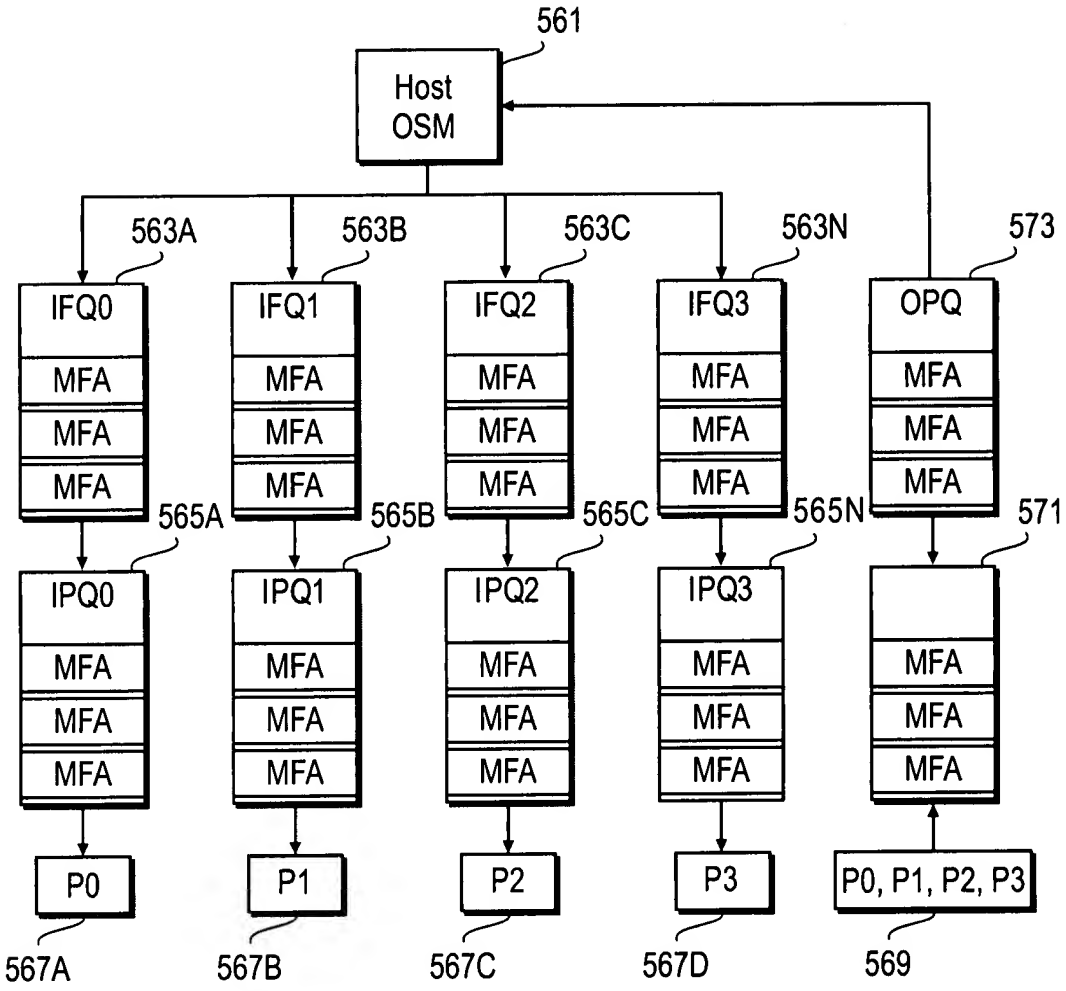


FIG. 13 I2O free and post queues in MSoC

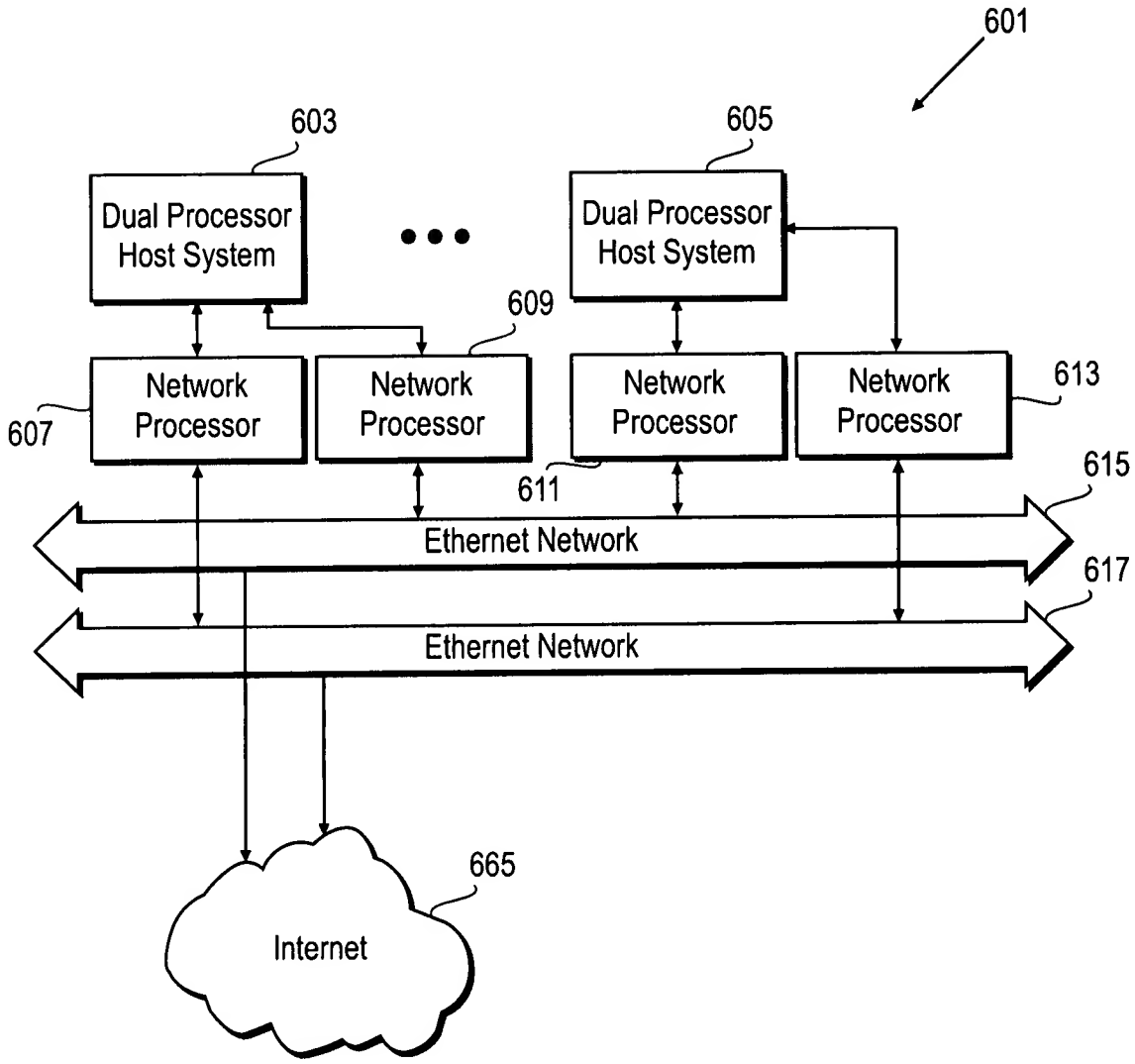

601
603
605
Dual Processor Host System
Dual Processor Host System
609
Network Processor
Network Processor
Network Processor
Network Processor
607
613
611
615
Ethernet Network
617
Ethernet Network
665
Internet

FIG. 14

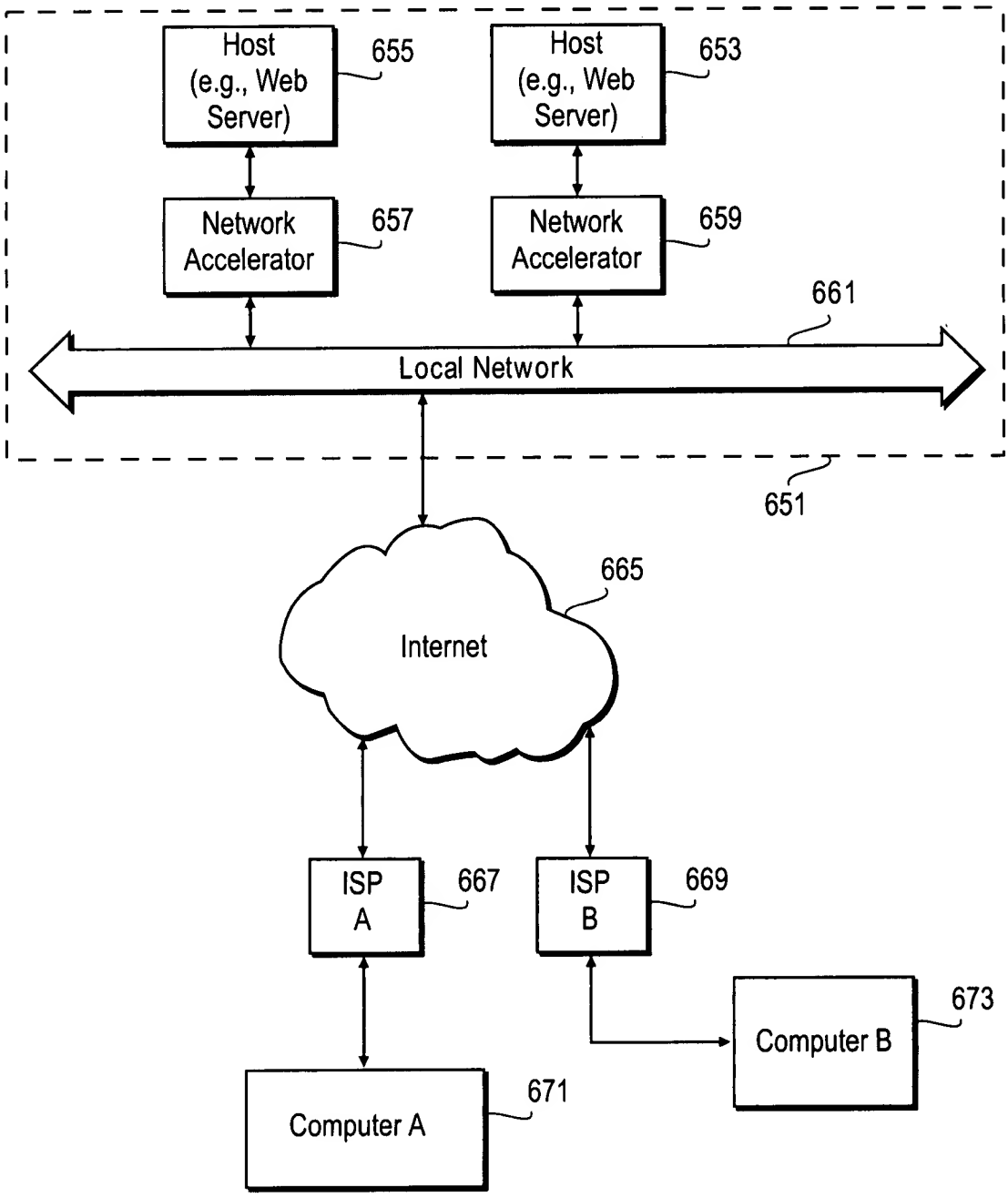

Host
(e.g., Web
Server)
655
Host
(e.g., Web
Server)
653
Network
Accelerator
657
Network
Accelerator
659
661
Local Network
651
665
Internet
ISP
A
667
ISP
B
669
673
Computer B
671
Computer A

FIG. 15

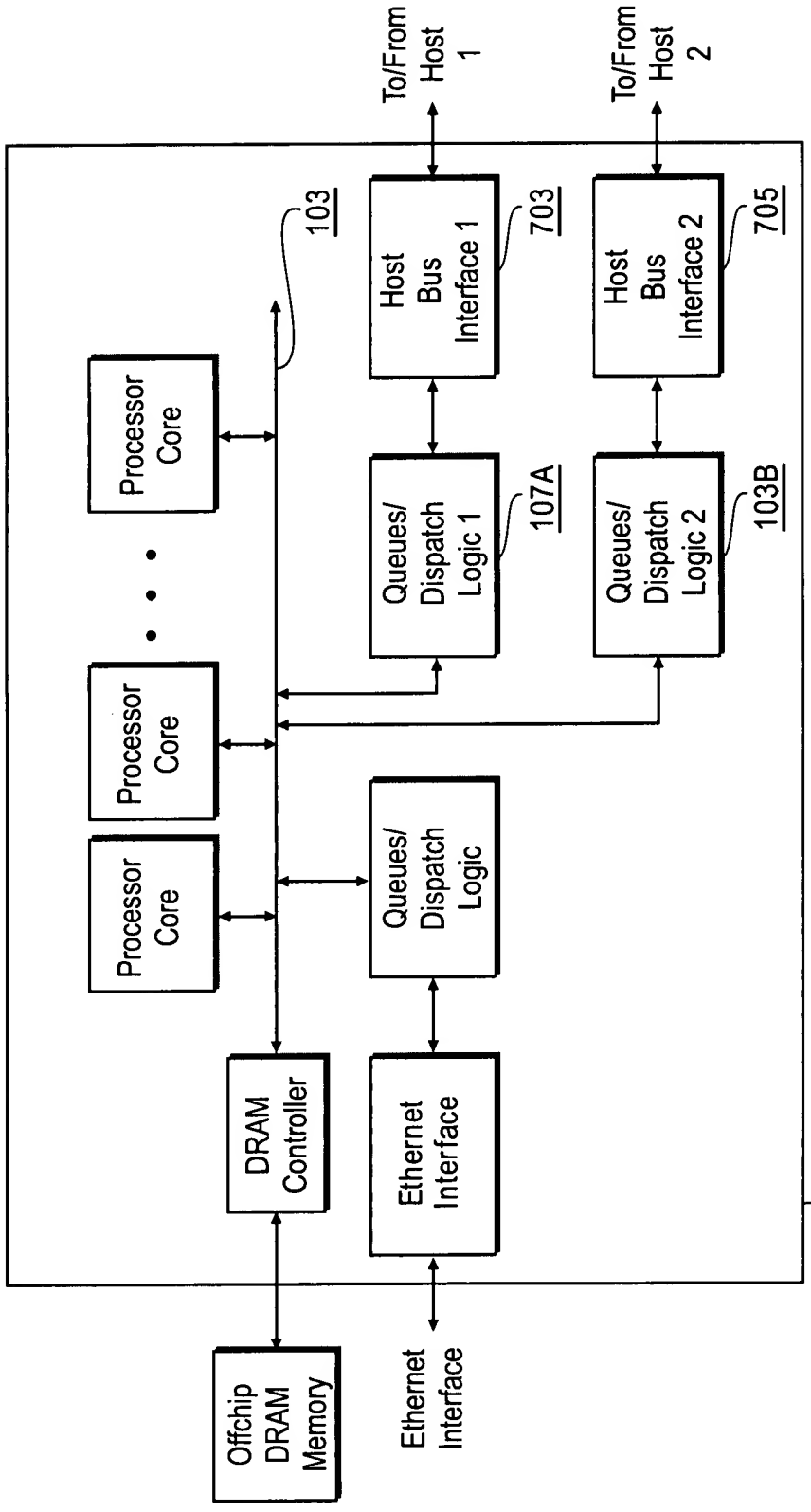
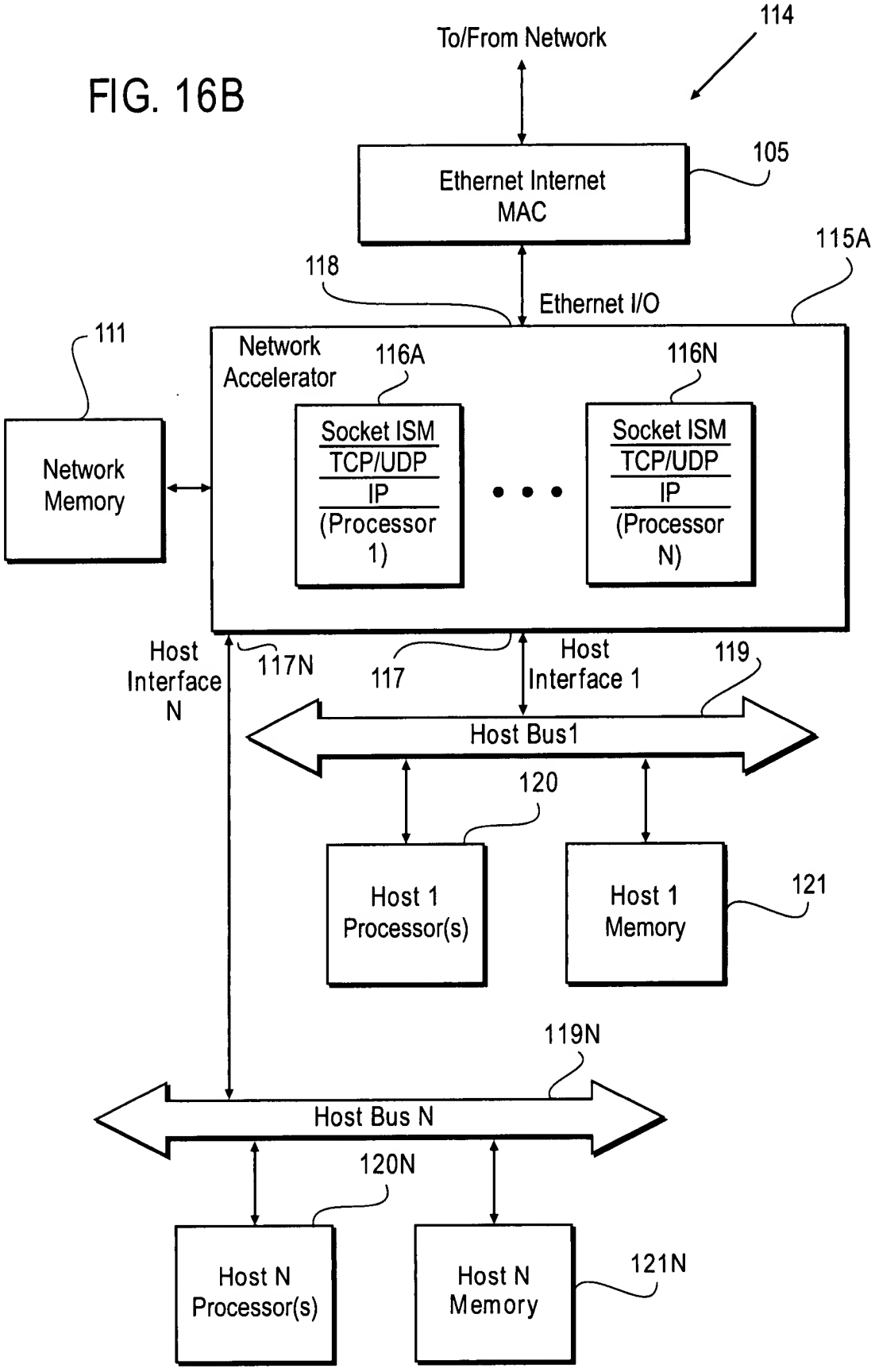

To/From Host 1
To/From Host 2
103
Host Bus Interface 1
703
Host Bus Interface 2
705
Processor Core
Processor Core
Processor Core
Queues/ Dispatch Logic 1
107A
Queues/ Dispatch Logic 2
103B
Queues/ Dispatch Logic
DRAM Controller
Ethernet Interface
Offchip DRAM Memory
Ethernet Interface
701

FIG. 16A

FIG. 16B


114
To/From Network
Ethernet Internet MAC
105
115A
118
Ethernet I/O
111
Network Accelerator
116A
116N
Network Memory
Socket ISM
TCP/UDP
IP
(Processor 1)
Socket ISM
TCP/UDP
IP
(Processor N)
Host Interface N
117N
117
Host Interface 1
119
Host Bus1
120
Host 1 Processor(s)
Host 1 Memory
121
119N
Host Bus N
120N
Host N Processor(s)
Host N Memory
121N

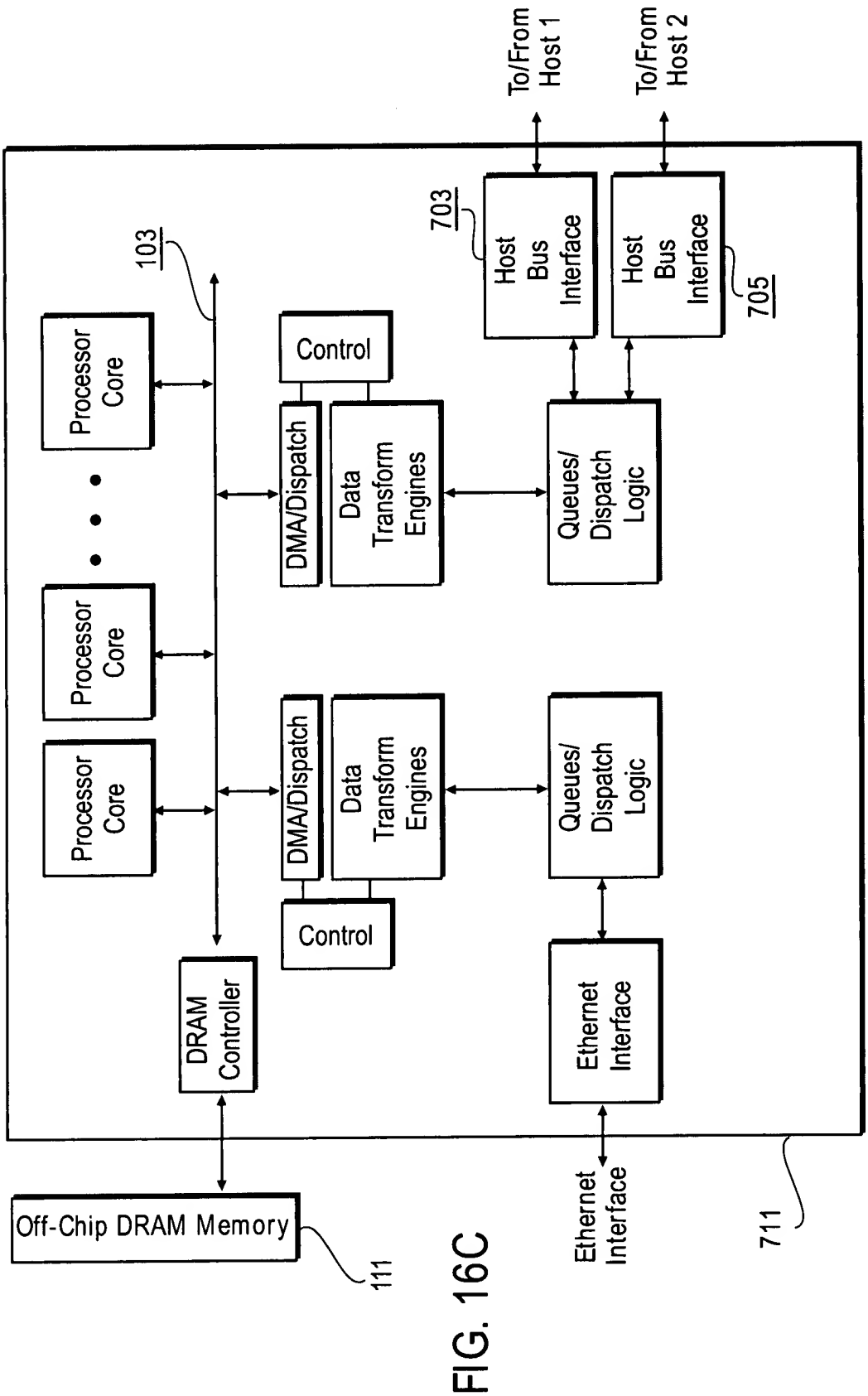

To/From Host 1
To/From Host 2
703
Host Bus Interface
Host Bus Interface
705
103
Processor Core
Processor Core
Processor Core
Control
DMA/Dispatch
Data Transform Engines
Queues/ Dispatch Logic
DMA/Dispatch
Data Transform Engines
Queues/ Dispatch Logic
Control
DRAM Controller
Ethernet Interface
Off-Chip DRAM Memory
111
Ethernet Interface
711

FIG. 16C

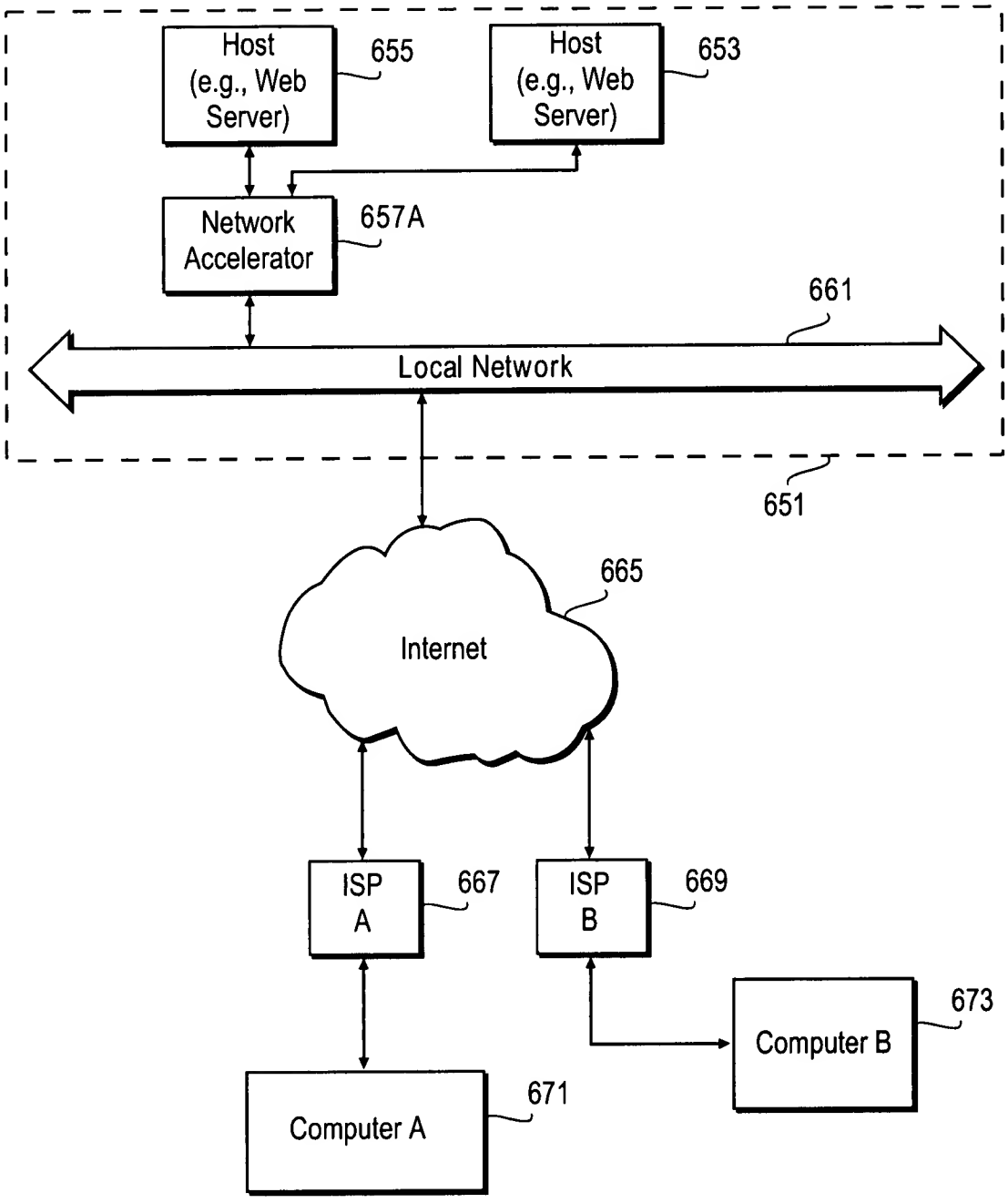

Host
(e.g., Web
Server)
655
Host
(e.g., Web
Server)
653
Network
Accelerator
657A
661
Local Network
651
665
Internet
ISP
A
667
ISP
B
669
673
Computer B
671
Computer A

FIG. 16D

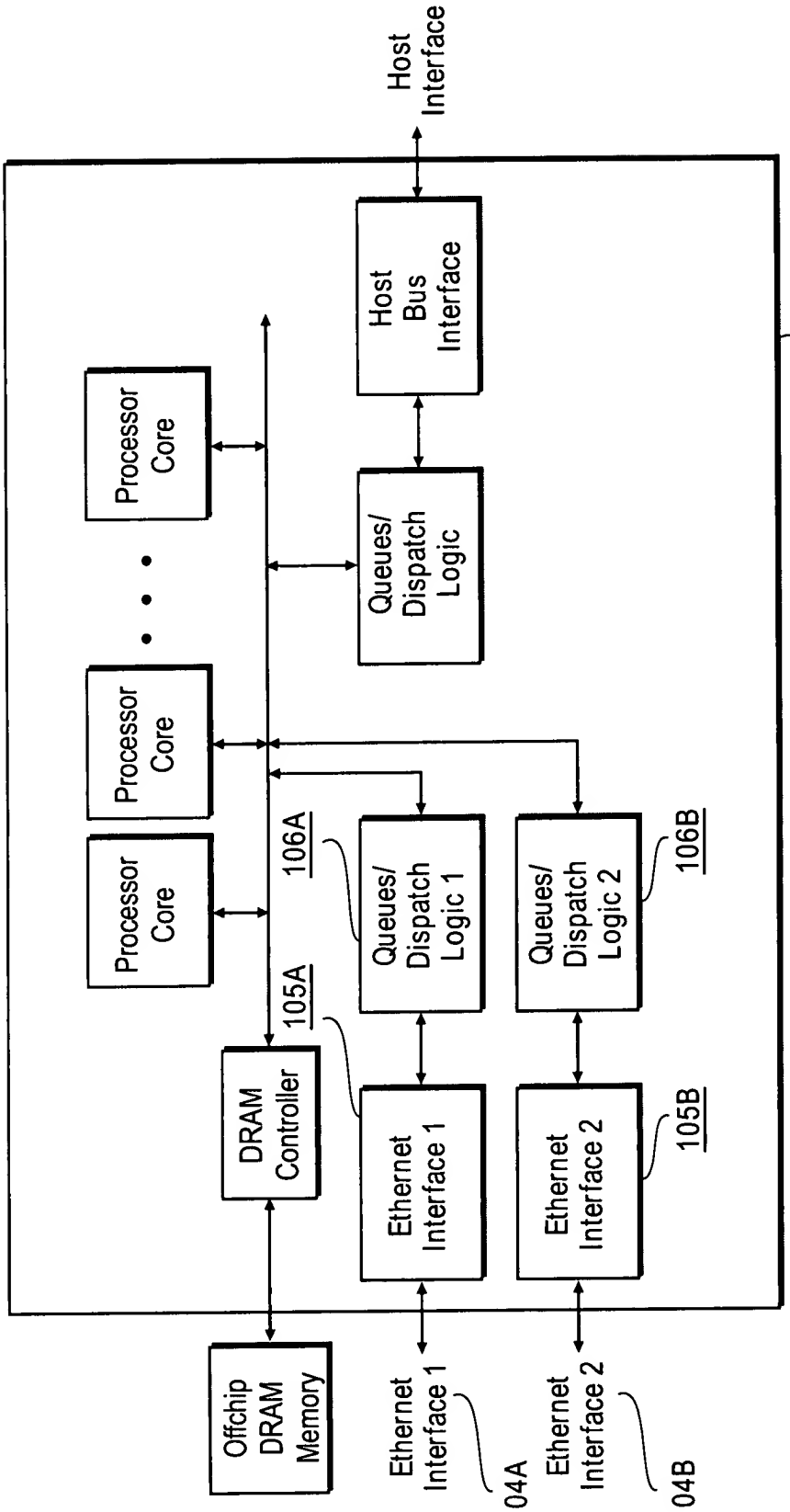

Host Interface
Host Bus Interface
Processor Core
Processor Core
Processor Core
Queues/ Dispatch Logic
Queues/ Dispatch Logic 1
Queues/ Dispatch Logic 2
106A
106B
DRAM Controller
105A
Ethernet Interface 1
Ethernet Interface 2
105B
Offchip DRAM Memory
Ethernet Interface 1
104A
Ethernet Interface 2
104B
751

FIG. 17A

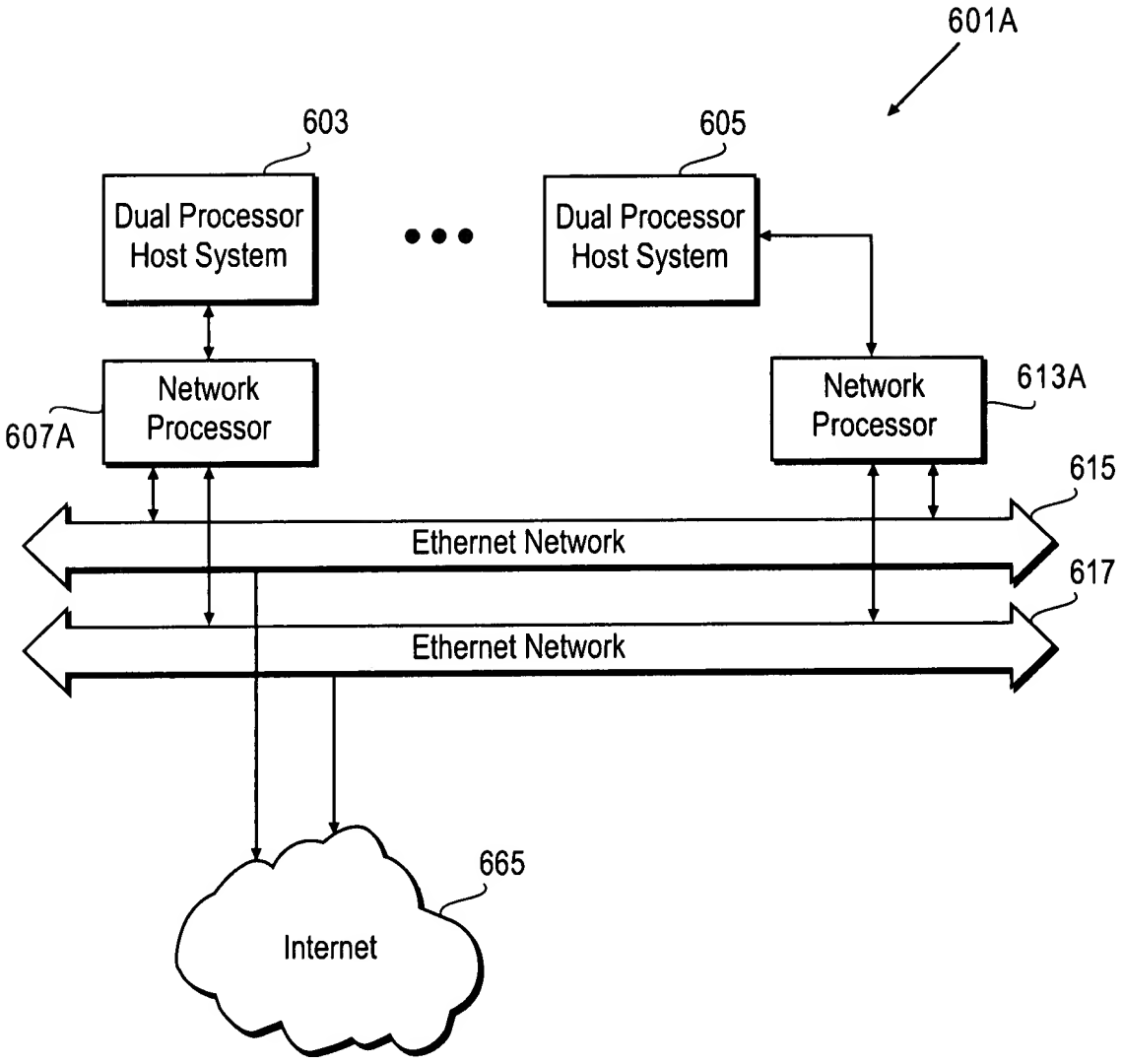

601A
603
605
Dual Processor Host System
Dual Processor Host System
Network Processor
607A
Network Processor
613A
615
Ethernet Network
617
Ethernet Network
665
Internet

FIG. 17B

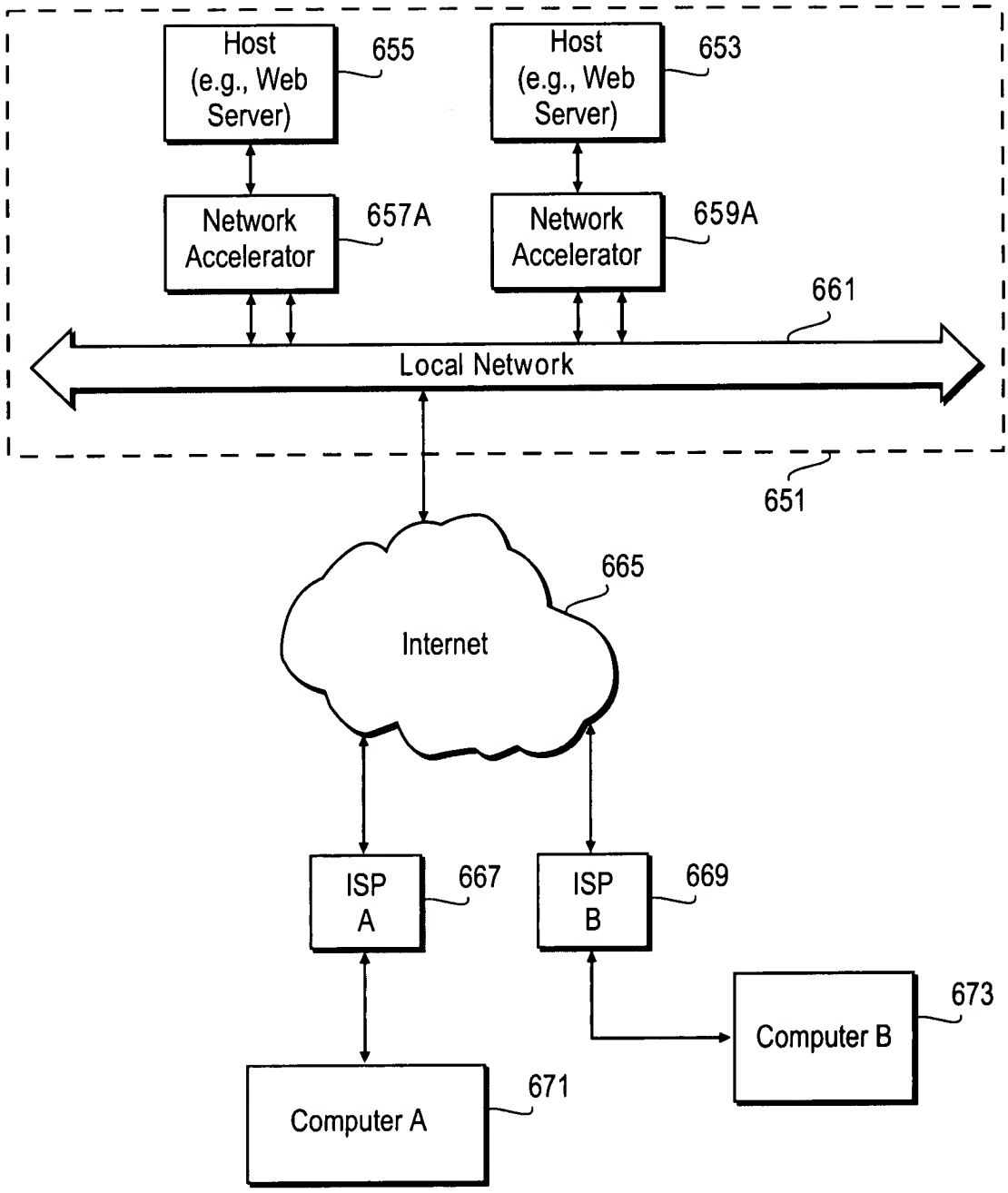

Host
(e.g., Web
Server)
655
Host
(e.g., Web
Server)
653
Network
Accelerator
657A
Network
Accelerator
659A
661
Local Network
651
665
Internet
ISP
A
667
ISP
B
669
673
Computer B
671
Computer A

FIG. 17C